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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
TABONE JR, JOHN J

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,646	KLEVELAND ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _01 September 2005_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-43_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-43_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _21 October 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _090/2005_.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-43 remain pending in the current application. Claims 1, 18 and 36 have been amended. Claims 44-47 have been cancelled.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/01/2005 has been entered.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 18 and 36 have been considered but are moot in view of the new ground(s) of rejection.

<u>As per arguments for independent claims 1, 18 and 36:</u>

The Applicants argues in paragraph 1, page 10 of the Remarks “Claims 1, 18, and 36 to specify that the recited redundancy acts occur when field programming the memory array - not when testing the memory array” and “Fujisaki fails to anticipate the claims and that one skilled in the art would not have been motivated to modify Fujisaki to yield the claimed invention because Fujisaki teaches away from such a modification”.

The Examiner disagrees with the Applicants' statements. Claims 1, for instance, recites, "in response to an error in writing the primary block when field programming the memory array...writing to the redundant block". By this the "redundancy acts" happen as a result of finding an error when writing to the primary block. The Examiner asserts that "redundancy acts" are performed as a result of testing or finding an error in the defective cell ("in response to an error") then reconfiguring the memory array to write to the redundant cell instead. It is also not clearly written in the claim language of claims 1, 18 and 36 how the error is found in "writing the primary block when field programming the memory array".

Further, the Examiner contends that writing to the memory array and field programming the memory are two different operations. The Examiner does not know, by the claims language, if the error occurs in writing the memory array or field programming the array. This must be clarified in response to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1 and 18 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: in response to an error in writing the primary block implies that a testing step was performed, but is missing from the claim. The "redundancy acts" are typically performed as a result of testing or finding an

error in the defective cell ("in response to an error") then reconfiguring the memory array to write to the redundant cell instead.

5. Claim 36 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: elements that provide the testing step to find the error and response to the error.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 10, 12, 15,16, 18-20, 22, 23, 25-29, and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisaki (US-5831989), hereinafter Fujisaki, in view of Pekny (US-6553510), hereinafter Pekny.

<u>Claim 1:</u>

Fujisaki teaches of a redundancy-structured memory under tested MUT has, in addition to a memory cell array (primary block) MCA, row address relief lines SR and column address relief lines SC formed on the periphery of the memory cell array MCA (redundant block of memory cells). Fujisaki also teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (storing a flag and

writing to the redundant block) as that of the memory cell which failed. (Col. 2, lines 10-23, Fig. 6). Fujisaki does not explicitly teach "the set of memory cells is in the memory array". However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine or make integral Fujisaki's failure analysis memory and MUT. The artisan would have been motivated to do so since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *In re Larson*, 144 USPQ 347 (CCPA 1965).

Fujisaki does not explicitly teach "field programming the memory array". However, Fujisaki does teach a memory testing apparatus for testing a semiconductor integrated circuit memory. (Col. 1, lines 6-10). Pekny teaches in an analogous art the present invention performs the redundant programming after the memory device is packaged and while the memory device is in operation (field programming the memory array). Further, Pekny teaches the present invention can be implemented <u>in any memory device</u> and is not limited to non-volatile memory devices such as flash memories, but can be incorporated in any memory device including DRAM, SRAM, SDRAM <u>or the like</u>. (Col. 5, ll. 19-37, col. 7, ll. 14-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisaki's memory array to adopt Pekny's field programming capabilities. The artisan would be motivated to do so because fabrication and environmental variables often result in single member cell failures, which are not easily identified prior to packaging, and Fujisaki's memory array can be re-programmed such that available redundant memory

cell locations are programmed to replace a location including a defective memory cell in the field.

Claim 2:

Fujisaki teaches that if a failure occurs during a memory test (reading the primary block), the failure signal (flag) is written in an address of the flag memory corresponding to the address of the memory under test MUT. Fujisaki further discloses at the time of carrying out the failure relief analysis for a tested memory, it is sufficient to read out only the contents of one or more memory blocks corresponding to one or more flag addresses in which a flag of logical "1" has been stored. (Col. 10, lines 13-15; col. 12, lines 24-39).

Claims 3:

Fujisaki teaches that of the memory under test is subdivided in its memory area into a plurality of memory blocks (plurality of smaller blocks). Fujisaki also teaches during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell (error in writing at least one bit in the smaller block of the primary block) is written in the same address of the failure analysis memory 5. (Col. 2, lines 19-22; col. 12, lines 28,29).

Claims 4:

Fujisaki teaches that the failure analysis memory 5 is subdivided (smaller blocks) into memory blocks of 2^6 (oct-byte) in the row direction, 2^6 in the column direction, and the total 4096 (2^6 X 2^6) (page) memory blocks.

Claims 10:

Fujisaki teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (direct mapping) as that of the memory cell which failed. (Col. 2, lines 10-23, Fig. 6).

Claim 12:

Fujisaki teaches as a result of detecting failed cells in the memory under test MUT the defective cell can be replaced by any one of the cells (full-associative mapping) of the address relief lines SR or SC. (Col. 2, lines 10-23, Fig. 6).

Claim 15:

Fujisaki teaches a memory testing apparatus for testing a semiconductor integrated circuit memory (semiconductor material). (Col. 1, lines 6-10).

Claim 16:

Fujisaki teaches a flag memory FLM where a flag is stored to indicate the address of the memory under test MUT where the failure has occurred. (Col. 10, lines 17-21).

Claim 18:

Fujisaki teaches of a redundancy-structured memory under tested MUT has, in addition to a memory cell array (primary block) MCA, row address relief lines SR and column address relief lines SC formed on the periphery of the memory cell array MCA (redundant block of memory cells). Fujisaki also teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory

cell is written in the same address of the failure analysis memory 5 (storing a flag and writing to the redundant block) as that of the memory cell which failed. (Col. 2, lines 10-23, Fig. 6). Fujisaki does not explicitly teach “field programming the memory array”. However, Fujisaki does teach a memory testing apparatus for testing a semiconductor integrated circuit memory. (Col. 1, lines 6-10). Pekny teaches in an analogous art the present invention performs the redundant programming after the memory device is packaged and while the memory device is in operation (field programming the memory array). Further, Pekny teaches the present invention can be implemented in any memory device and is not limited to non-volatile memory devices such as flash memories, but can be incorporated in any memory device including DRAM, SRAM, SDRAM or the like. (Col. 5, ll. 19-37, col. 7, ll. 14-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisaki's memory array to adopt Pekny's field programming capabilities. The artisan would be motivated to do so because fabrication and environmental variables often result in single member cell failures, which are not easily identified prior to packaging, and Fujisaki's memory array can be re-programmed such that available redundant memory cell locations are programmed to replace a location including a defective memory cell in the field.

Claim 19:

Fujisaki teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (storing a flag in response to the error in

writing to the primary block) as that of the memory cell which failed. (Col. 2, lines 10, 23).

Claim 20:

Fujisaki teaches a flag memory FLM where a flag is stored to indicate the address of the memory under test MUT where the failure has occurred. (Col. 10, lines 17-21).

Claim 22:

Fujisaki teaches that if a failure occurs during a memory test (reading the primary block), the failure signal (flag) is written in an address of the flag memory corresponding to the address of the memory under test MUT. Fujisaki further discloses at the time of carrying out the failure relief analysis for a tested memory, it is sufficient to read out only the contents of one or more memory blocks corresponding to one or more flag addresses in which a flag of logical "1" has been stored. (Col. 10, lines 13-15; col. 12, lines 24-39).

Claim 23:

Fujisaki teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (direct mapping) as that of the memory cell which failed. (Col. 2, lines 10-23, Fig. 6).

Claim 25:

Fujisaki teaches as a result of detecting failed cells in the memory under test MUT the defective cell can be replaced by any one of the cells (full-associative mapping) of the address relief lines SR or SC. (Col. 2, lines 10-23, Fig. 6).

Claim 26:

Fujisaki teaches that the failure analysis memory 5 comprises an address formatter FOM_1 (redundancy address matching circuit) for matching an address of a failure memory cell in a memory under test MUT (primary block) with an address of the failure analysis memory 5. (Col. 3, lines 22-25).

Claim 27:

Fujisaki teaches the failure analysis memory (redundant memory) which has the same storage capacity as the memory under test MUT is subdivided into a plurality of memory blocks and a flag memory. The failure data is written in an address in the failure analysis memory matching that as the MUT (determining the address is written...). Fujisaki teaches at the time the failure relief analysis for the tested memory is executed the contents of one or more memory blocks corresponding to one or more flag addresses is read out (reading the redundant memory). (Col. 12, lines 24,39).

Claim 28:

Fujisaki teaches that of the memory under test is subdivided in its memory area into a plurality of memory blocks (plurality of smaller blocks). Fujisaki also teaches during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell (error in writing at least one bit in the smaller block of

the primary block) is written in the same address of the failure analysis memory 5. (Col. 2, lines 19-22; col. 12, lines 28,29).

Claim 29:

Fujisaki teaches that the failure analysis memory 5 is subdivided (smaller blocks) into memory blocks of 2^6 (oct-byte) in the row direction, 2^6 in the column direction, and the total 4096 (2^6 X 2^6) (page) memory blocks.

Claim 35:

Fujisaki teaches a memory testing apparatus for testing a semiconductor integrated circuit memory (semiconductor material). (Col. 1, lines 6-10).

7. Claims 5-7, 17, 21 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisaki (US-5831989) in view of Creta et al. (US-6216247) and further in view of Pekny (US-6553510), hereinafter Pekny.

Claims 5 and 30:

Fujisaki does not explicitly teach "the error occurs when there is an error in writing a single bit". However, Fujisaki does teach during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell (error in writing at least one bit in the smaller block of the primary block) is written in the same address of the failure analysis memory 5. (Col. 2, lines 19-22). Creta teaches data from main memory 120 and its corresponding ECC value from the ECC memory is passed to a module/circuitry 112 that calculates a "syndrome" based upon the data and the ECC value. Creta also teaches that the syndrome indicates if there is an error and whether or

not it can be corrected. Creta discloses a syndrome value of "0" indicates that there is no error in the data. Creta further discloses a syndrome with an odd number of "1"s indicates that a single bit error has occurred. (Col. 3, lines 40-52). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisaki's memory testing apparatus to include Creta's ECC memory 125 and module 112. The artisan would have been motivated to do so because this would enable Fujisaki to calculate ECC syndromes and detect single bit errors.

Claims 6 and 31:

The motivation to combine Fujisaki in view of Creta is per claims 5 and 30 above. Creta teaches if the syndrome contains an even number of zeroes, there is a double bit error. (Col. 3, lines 49-51).

Claims 7 and 32:

The motivation to combine Fujisaki in view of Creta is per claims 5 and 30 above. Creta teaches if the syndrome contains an even number of zeroes, there is a double bit or more error which can be detected but cannot be corrected (uncorrectable error). (Col. 3, lines 49-51).

Claims 17 and 21:

The motivation to combine Fujisaki in view of Creta is per claims 5 and 30 above. Creta teaches the use of sending a flag to the processor (host device) in the enhanced memory controller 500 when a memory error has occurred. The processor can then take measures to correct the fault with ECC technology.

8. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisaki (US-5831989) in view of Rosen (US-6026476), and further in view of Pekny (US-6553510), hereinafter Pekny.

<u>Claims 11, 24:</u>

Fujisaki does not explicitly teach set-associative mapping. However, Fujisaki does teach of direct and full-associative mapping per rejection of claims 10 and 23 and 12 and 25, respectively above. Fujisaki teaches that this is accomplished via the failure relief analyzer 6, which includes the failure analysis memory 6. (Col. 3, lines 19-28). Rosen teaches of a translation lookaside buffer TLB 22 which can be mapped in accordance with any one of a number of possible mapping policies such as, direct mapping, <u>set-associative mapping</u>, or full-associative mapping. Rosen teaches the TLB 22 simultaneously compares an input address to the virtual address tags in each and every tag line in tag array 23 for full-associative mapping. For <u>set-associative mapping</u> an input address is compared to a set of virtual address tags. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisaki's failure relief analyzer 6 to incorporate Rosen's translation lookaside buffer TLB 22 in the address formatter section. The artisan would have been motivated to do so because this would enable Fujisaki to have more versatility in mapping the addresses which are written to the failure analysis memory 6 (redundant memory) via a predefined set of addresses

9. Claim 8, 9, 13, 14, 33, 34, 36-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisaki (US-5831989), hereinafter Fujisaki, in view of Matsumoto et al. (US- 5278839), hereinafter Matsumoto, and further in view of Pekny (US-6553510), hereinafter Pekny.

Claim 36:

Fujisaki teaches of a redundancy-structured memory under tested MUT has, in addition to a memory cell array (primary block) MCA, row address relief lines SR and column address relief lines SC formed on the periphery of the memory cell array MCA (redundant block of memory cells). Fujisaki also teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (storing a flag and writing to the redundant block) as that of the memory cell which failed. (Col. 2, lines 10, 23). Fujisaki does not explicitly teach the type of memory. However, Fujisaki does teach a memory testing apparatus for testing a semiconductor integrated circuit memory. (Col. 1, lines 6-10). Matsumoto suggests the use of a bipolar PROM (programmable read-only memory) as the memory array (programmable memory cells). (Col. 9, lines 4-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Fujisaki's memory array with Matsumoto's PROM. The artisan would have been motivated to do so because a bipolar PROM transistor 40 can reduce the size of layout of the memory array, thus saving cost of manufacture.

Fujisaki does not explicitly teach "field programming the memory array". However, Fujisaki does teach a memory testing apparatus for testing a semiconductor

integrated circuit memory. (Col. 1, lines 6-10). Pekny teaches in an analogous art the present invention performs the redundant programming after the memory device is packaged and while the memory device is in operation (field programming the memory array). Further, Pekny teaches the present invention can be implemented in any memory device and is not limited to non-volatile memory devices such as flash memories, but can be incorporated in any memory device including DRAM, SRAM, SDRAM or the like. (Col. 5, ll. 19-37, col. 7, ll. 14-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Fujisaki's memory array to adopt Pekny's field programming capabilities. The artisan would be motivated to do so because fabrication and environmental variables often result in single member cell failures, which are not easily identified prior to packaging, and Fujisaki's memory array can be re-programmed such that available redundant memory cell locations are programmed to replace a location including a defective memory cell in the field.

Claim 37:

Fujisaki teaches that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 (storing a flag in response to the error in writing to the primary block) as that of the memory cell which failed. (Col. 2, lines 10, 23).

Claim 38:

Fujisaki teaches that if a failure occurs during a memory test (reading the primary block), the failure signal (flag) is written in an address of the flag memory corresponding

to the address of the memory under test MUT. Fujisaki further discloses at the time of carrying out the failure relief analysis for a tested memory, it is sufficient to read out only the contents of one or more memory blocks corresponding to one or more flag addresses in which a flag of logical "1" has been stored. (Col. 10, lines 13-15; col. 12, lines 24-39).

Claim 39:

Fujisaki teaches that the failure analysis memory 5 comprises an address formatter FOM_1 (redundancy address matching circuit) for matching an address of a failure memory cell in a memory under test MUT (primary block) with an address of the failure analysis memory 5. (Col. 3, lines 22-25).

Claims 8 and 40:

Fujisaki does not explicitly teach "while attempting to program the memory cell, determining that the memory cell is not programmed". However, Fujisaki does teach that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 as that of the memory cell which failed. (Col. 2, lines 10, 23). Matsumoto suggests the use of a bipolar PROM (programmable read-only memory) as the memory array (programmable memory cells) which is the junction shorting type. Matsumoto teaches that the non-written state of the transistor 40 corresponds to the fused state of the fuse (not in a programmed state). (Col. 9, lines 4-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Fujisaki's memory array with Matsumoto's PROM. The artisan would have been motivated to do

so because programming the bipolar PROM transistor 40 can control the level of the output signal 49 of the programmable fuse.

Claims 9 and 41:

Fujisaki does not explicitly teach "reading the memory cell after the attempt to program the memory cell; and determining that the memory cell is not programmed. However, Fujisaki does teach that during a test of a memory under test MUT, a failure data of, for example, logical "1" indicating failure of a memory cell is written in the same address of the failure analysis memory 5 as that of the memory cell which failed. (Col. 2, lines 10, 23). Matsumoto suggests the use of a bipolar PROM (programmable read-only memory) as the memory array (programmable memory cells) which is the junction shorting type. Matsumoto teaches that the written state of the transistor 40 corresponds to the non-fused state of the fuse (programmed state). Matsumoto teaches a control signal 48 is set at a low level when the redundancy repair is required (after reading the cell). (Col. 9, lines 4-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Fujisaki's memory array with Matsumoto's PROM. The artisan would have been motivated to do so because programming the bipolar PROM transistor 40 can control the level of the output signal 49 of the programmable fuse and the programmed state of the transistor 40 can be determined.

Claim 43:

Fujisaki teaches a memory testing apparatus for testing a semiconductor integrated circuit memory (semiconductor material). (Col. 1, lines 6-10).

Claims 13, 33 and 42:

Fujisaki does not explicitly teach the type of memory. However, Fujisaki does teach a memory testing apparatus for testing a semiconductor integrated circuit memory. (Col. 1, lines 6-10). Matsumoto suggests the use of a bipolar PROM (programmable read-only memory) as the memory array (write-once memory cells). (Col. 9, lines 4-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Fujisaki's memory array with Matsumoto's PROM. The artisan would have been motivated to do so because a bipolar PROM transistor 40 can reduce the size of layout of the memory array, thus saving cost of manufacture.

Claims 14 and 34:

Fujisaki does not explicitly teach the type of memory. However, Fujisaki does teach a memory testing apparatus for testing a semiconductor integrated circuit memory. (Col. 1, lines 6-10). Matsumoto suggests the use of a bipolar PROM (programmable read-only memory) as the memory array (programmable memory cells). (Col. 9, lines 4-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace Fujisaki's memory array with Matsumoto's PROM. The artisan would have been motivated to do so because a bipolar PROM transistor 40 can reduce the size of layout of the memory array, thus saving cost of manufacture.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr. 11/21/05
John J. Tabone, Jr.
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER